

## FACSIMILE

Page 4

## PROPOSED CLAIM AMENDMENTS

1. (PROPOSED) A memory device having plural DRAM sub-arrays, each with plural array rows, comprising:

an address decoder for decoding an address of a memory access request and indicating which of the plural DRAM sub-arrays are referenced by the memory access request; and

refresh circuitry, responsive to the indication of the address decoder, to refresh at least one array row of at least one of the plural DRAM sub-arrays not referenced by the memory access request while contemporaneously performing the memory request, wherein logically adjacent rows are placed in different sub-arrays,

wherein a first row is in a first sub-array and a second row is in a second sub-array, the second row being one logical row from the first row, and a third row is in the first sub-array and a fourth row is in the second sub-array, the fourth row being one logical row from the third row, wherein the first row is not logically adjacent to the third row.

11. (PROPOSED) A method of refreshing a memory device having a plural DRAM sub-arrays, each with plural array rows, the method comprising:

(a) placing logically adjacent rows in different sub-arrays, wherein a first row is in a first sub-array and a second row is in a second sub-array, the second row being one logical row from the first row, and a third row is in the first sub-array and a fourth row is in the second sub-array, the fourth row being one logical row from the third row, wherein the first row is not logically adjacent to the third row;

(b) decoding an address of a memory request;

(c) indicating which of the plural DRAM sub-arrays are referenced by the memory access request;

(d) refreshing, in response to the indicating step, at least one array row of at least one of the plural DRAM sub-arrays not referenced by the memory access request; and

(e) executing the memory address request,

wherein steps (d) and (e) are performed contemporaneously.

## FACSIMILE

Page 5

28. (PROPOSED) A memory device having plural DRAM sub-arrays, each with plural array rows, comprising:

an address decoder for decoding an address of a memory access request and indicating which of the plural DRAM sub-arrays are referenced by the memory access request; and

refresh circuitry, responsive to the indication of the address decoder, to refresh at least one array row of at least one of the plural DRAM sub-arrays not referenced by the memory access request while contemporaneously performing the memory request, wherein logically adjacent rows are placed in different sub-arrays, and the logically adjacent rows in different sub-arrays comprise rows other than the last and first rows of consecutive sub-arrays, wherein each sub-array includes rows that are not logically adjacent.

30. (PROPOSED) A method of refreshing a memory device having a plural DRAM sub-arrays, each with plural array rows, the method comprising:

(a) placing logically adjacent rows in different sub-arrays, and the logically adjacent rows in different sub-arrays comprise rows other than the last and first rows of consecutive sub-arrays, wherein each sub-array includes rows that are not logically adjacent;

(b) decoding an address of a memory request;

(c) indicating which of the plural DRAM sub-arrays are referenced by the memory access request;

(d) refreshing, in response to the indicating step, at least one array row of at least one of the plural DRAM sub-arrays not referenced by the memory access request; and

(e) executing the memory address request,

wherein steps (d) and (e) are performed contemporaneously.